

## **Amendments In The Claims**

### **Currently Pending Claims**

- 1.(currently amended)            A method of testing a memory under test on a memory tester, the method  
2 comprising the steps of:
- 4            (a)            applying the same sequence of transmit vectors to the memory under test and to a  
6                        work memory within the memory tester, the sequence of transmit vectors causing  
                             the storing of test pattern data within the memories to which it is applied, the stored  
                             test pattern data in each memory being an end result remaining stored therein after  
                             the conclusion of the application of the entire sequence of transmit vectors; and  
8            (b)            subsequent to the conclusion of step (a), comparing the test pattern data content of  
                             the memory under test with the test pattern data content of the work memory.
- 2.(original)            A method as in claim 1 wherein the same sequence of transmit vectors is an instance  
2 of that sequence that is applied simultaneously to the memory under test and to the work memory.
- 3.(original)            A method as in claim 1 wherein the same sequence of transmit vectors is separate  
2 instances of that sequence that are applied at different times to the memory under test and to the work  
memory.
- 4.(original)            A method as in claim 1 wherein the work memory is a selectable portion of an  
2 interior test memory within the memory tester.
- 5.(original)            A method as in claim 4 further comprising the step of interleaving work memory  
2 transactions among banks of DRAM.
- 6 .(previously amended)            A method as in claim 4 further comprising the step of storing comparison  
2 results from step (b) in an error catch memory that is a portion of an interior test memory within the  
memory tester.

4 7.(original) A method as in claim 6 further comprising the step of interleaving error catch  
memory transactions among banks of DRAM.

8.(original) A method as in claim 4 wherein the interior test memory is comprised of a plurality  
2 of memory sets and the selectable portion is a segment of a memory set.

9.(original) A method as in claim 8 further comprising the step of storing comparison results  
2 from step (b) in an error catch memory that is a portion of a memory set different than the memory set  
of which the work memory is a segment.

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